REMARKS

Prior to this preliminary amendment, claims 1-29 were pending in the present application. By this preliminary amendment, Applicant has added new claims 30-39. As such, claims 1-39 are now pending in the present application. Applicant has also amended the specification by deleting a few lines in the detailed description. By deleting those few lines, Applicant has not introduced any new matter herein and has solely improved the readability of the detailed description.

Applicant respectfully requests an early consideration and examination of pending claims 1-39. If the Examiner has any questions or comments, he or she is encouraged to call the undersigned Applicant's attorney.

Respectfully Submitted;
FARJAMI & FARJAMI LLP

Michael Farjami, Esq.
Reg. No. 38,135

Michael Farjami, Esq.
FARJAMI & FARJAMI LLP
16148 Sand Canyon
Irvine, California 92618
Telephone: (949) 784-4600
Facsimile: (949) 784-4601

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed: Commissioner of Patents and Trademarks; Washington, D.C. 20231

Date of Deposit: 3/5/2001

Sara Ansari
Name of Person Signing

Sara Ansari
Signature Date

generator 230 also functions to generate the signals for proper encoding pixel data 228 in SVGA video format into, for example, NTSC video format. Modulator/timing generator 230 operates at the frequency of clock 278, for example, at 50 MHz in the present embodiment of the invention's video encoder 202. Modulator/timing generator 230 provides its output 232 to the invention's DAC interface 236.

DAC interface 236 digitally adds or combines the format data information with the appropriate level information for that format, and provides this information to an external device, such as a television monitor. DAC interface 236 provides outputs 238, 240, 242, and 244, respectively, to DACs 246, 248, 250, and 252. DACs 246, 248, 250, and 252 convert the digital data they receive at outputs 238, 240, 242, and 244, respectively, into analog data.

Referring to Figures 3A and 3B, the operation of the present embodiment's FIFO 326, corresponding to FIFO 226 in Figure 2, is now discussed in more detail. FIFO 326 receives clock 376, corresponding to clock 276 in Figure 2. Clock waveform 376 in Figure 3B corresponds to clock 376 in Figure 3A. Pixel data waveform 322 in Figure 3B corresponds to pixel data 322 in Figure 3A which in turn corresponds to pixel data 222 in Figure 2. Clock waveform 378 in Figure 3B corresponds to clock 378 in Figure 3A. Pixel data waveform 328 in Figure 3B corresponds to pixel data 328 in Figure 3A which in turn corresponds to pixel data 228 in Figure 2.

~~[NOTE: The line is written into the FIFO one pixel per clock on consecutive clocks (e.g. 1024 consecutive clocks), thus about two lines (e.g. 2.66 lines) are not clocked into the FIFO. This line is read out of the FIFO on every other clock. So one~~

A ~~[illegible] "burst" into the FIFO, and then gradually read out. The next section needs to be~~
A ~~rewritten to reflect this (i.e. the data is [illegible] on every third clock).]; Q: What is~~
A ~~clocked out of FIFO, is it P1, P3, P5, etc. . . or P1, P4, P7, etc . . .~~

At time 388, which corresponds to the beginning of a first clock cycle in clock waveform 376, one pixel in a line of pixel data, shown as "Pixel 1" in pixel data waveform 322, is written into FIFO 326. More precisely, the pixel written into FIFO 326 is written into FIFO 326 upon a falling edge of clock waveform 376. In the present example, "Pixel 1" in a line of pixel data is written into FIFO 326 on edge 302 which is the falling edge occurring at time 388 in clock waveform 376.

At time 390, which corresponds to the beginning of a second clock cycle in clock waveform 376, "Pixel 2" in the line of pixel data is written into FIFO 326. Similarly, at time 392, which corresponds to the beginning of a third clock cycle of clock waveform 376, "Pixel 3" in the line of pixel data is written into FIFO 326. . More precisely, each pixel in the line of pixel data written into FIFO 326 is written into FIFO 326 upon a falling edge of clock waveform 376. In the present example, "Pixel 4" of the line of pixel data is written into FIFO 326 on edge 303 which is the falling edge occurring at time 394 in clock waveform 376. Thus, in the present embodiment's invention, each pixel (i.e., "Pixel 1," "Pixel 2," "Pixel 3," etc.) in the line of pixel data is written into FIFO 326 on the falling edge of every clock cycle of clock waveform 376 in Figure 3B. After the last pixel in the line of pixel data is written into FIFO 326, the next approximately 2.66 lines of pixel data are not written into FIFO 326.

As shown in Figure 3B, between time 388 and time 394, there are two clock cycles

generator 230 also functions to generate the signals for proper encoding pixel data 228 in SVGA video format into, for example, NTSC video format. Modulator/timing generator 230 operates at the frequency of clock 278, for example, at 50 MHz in the present embodiment of the invention's video encoder 202. Modulator/timing generator 230 provides its output 232 to the invention's DAC interface 236.

DAC interface 236 digitally adds or combines the format data information with the appropriate level information for that format, and provides this information to an external device, such as a television monitor. DAC interface 236 provides outputs 238, 240, 242, and 244, respectively, to DACs 246, 248, 250, and 252. DACs 246, 248, 250, and 252 convert the digital data they receive at outputs 238, 240, 242, and 244, respectively, into analog data.

Referring to Figures 3A and 3B, the operation of the present embodiment's FIFO 326, corresponding to FIFO 226 in Figure 2, is now discussed in more detail. FIFO 326 receives clock 376, corresponding to clock 276 in Figure 2. Clock waveform 376 in Figure 3B corresponds to clock 376 in Figure 3A. Pixel data waveform 322 in Figure 3B corresponds to pixel data 322 in Figure 3A which in turn corresponds to pixel data 222 in Figure 2. Clock waveform 378 in Figure 3B corresponds to clock 378 in Figure 3A. Pixel data waveform 328 in Figure 3B corresponds to pixel data 328 in Figure 3A which in turn corresponds to pixel data 228 in Figure 2.

At time 388, which corresponds to the beginning of a first clock cycle in clock waveform 376, one pixel in a line of pixel data, shown as "Pixel 1" in pixel data waveform 322, is written into FIFO 326. More precisely, the pixel written into FIFO 326 is written into FIFO 326 upon a falling edge of clock waveform 376. In the present example, "Pixel 1" in a line of pixel data is written into FIFO 326 on edge 302 which is the falling edge occurring at time 388 in clock waveform 376.

At time 390, which corresponds to the beginning of a second clock cycle in clock waveform 376, "Pixel 2" in the line of pixel data is written into FIFO 326. Similarly, at time 392, which corresponds to the beginning of a third clock cycle of clock waveform 376, "Pixel 3" in the line of pixel data is written into FIFO 326. . More precisely, each pixel in the line of pixel data written into FIFO 326 is written into FIFO 326 upon a falling edge of clock waveform 376. In the present example, "Pixel 4" of the line of pixel data is written into FIFO 326 on edge 303 which is the falling edge occurring at time 394 in clock waveform 376. Thus, in the present embodiment's invention, each pixel (i.e., "Pixel 1," "Pixel 2," "Pixel 3," etc.) in the line of pixel data is written into FIFO 326 on the falling edge of every clock cycle of clock waveform 376 in Figure 3B. After the last pixel in the line of pixel data is written into FIFO 326, the next approximately 2.66 lines of pixel data are not written into FIFO 326.

As shown in Figure 3B, between time 388 and time 394, there are two clock cycles